REMARKS

Applicant appreciates the consideration of the present application. Applicant has amended Claim 19 to correct the inadvertent antecedent basis error in Claim 20 noted by the Examiner. Applicant respectfully traverses the rejections of Claims 1-5 and 23-26 based on U.S. Patent No. 6,067,260 to Ooishi et al. ("Ooishi") because, among other reasons, this reference describes selectively applying ***outputs*** from input output sense amplifiers having fixed connections to memory cells to global I/O lines to provide flexible redundancy, which contrasts with the selective connection of memory cells to a sense amplifier (i.e., to its input) as recited in independent apparatus Claim 1 and independent method Claim 23. Applicant further traverses the rejections of the several of the other claims for similar reasons. Reasons for patentability of the claims are discussed in detail below.

The § 112 rejections are overcome

Applicant has amended Claim 19 to replace "switch controller" with "input output control circuit." Applicant submits that this corrects the antecedent basis in Claim 20 error noted by the Examiner.

The rejections based on Ooishi should be withdrawn

Independent Claims 1 and 23 stand rejected under 35 U.S.C. § 102 as anticipated by Ooishi. Applicants respectfully point out that the grounds stated for the reject are inadequate in several ways. For example, the Office Action states that Ooishi teaches a memory device with primary and redundant memory cells, sense amplifiers connected to global input/output lines, and "a control circuit including switching circuit in figure 13 and multiplexer 618 in figure 12 for replacing a defective regular memory cell column with a redundant memory cell column" (Office Action, p. 3). However, the Office Action fails to indicate where Ooishi discloses or suggests, among other things, the following recitations of Claim 1:

> . . . an input output control circuit configurable to selectively connect input output lines to a sense amplifier such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input.

In fact, as shown in FIGs. 12 of Ooishi, the local I/O line pairs (M-I/O, RM-I/O), which come from sub I/O lines S-I/O that are connected to memory cells, are fixedly connected to respective sense amplifiers (608, 610, 612, 614, 616), and the ***outputs*** of the sense amplifiers are selectively connected to global I/O lines G-I/O by the I/O multiplexer 618. This sharply contrasts with the recitations of Claim 1, where memory cells are selectively connected to sense amplifiers (i.e., to the ***inputs*** of the sense amplifiers) by the input/output control circuit. For at least these reasons, Applicant submits that the rejections of Claims 1-5 are improper, and should be withdrawn. Applicant submits that the rejections of Claims 23-26 should be withdrawn for at least similar reasons.

Applicant submits that the rejections of Claims 6-22 should also be withdrawn because, among other reasons, Ooishi does not show the same I/O line configurations recited in these claims. For example, independent Claim 6 recites:

> . . . a plurality of input/output blocks being divided into first and second blocks and having a first local input/output line and ***a first global input/output line for the first block***, and a second local input/output line and ***a second global input/output line for the second block***,
>
> wherein data is input into and output from memory cells in the first block via the first local input/output line and the first global input/output line and data is input into and output from memory cells in the second block via the second local input/output line and the second global input/output line.

In other words, Claim 6 recites a configuration in which different blocks use different local and global I/O lines. In sharp contrast, the memory circuit described in the cited portions of Ooishi (FIGs. 11-13, column 16, line 27 through column 17, line 46) shows that the memory cells in regions 100a0, 100a1, SR0, SR1 use the ***same*** global I/O bus G-I/O (see, e.g., FIG. 12). For at least this reason, Applicant submits that

Ooishi does not disclose or suggest the recitations of independent Claim 6, and that the rejection of independent Claim 6 should, therefore, be withdrawn. Applicant submits that the rejection of independent Claim 15 should be withdrawn for at least similar reasons.

Applicant submits that dependent Claims 7-14 and 16-22 are patentable at least by virtue of the patentability of independent Claims 6 and 15. Applicant further submits that several of dependent Claims 7-14 and 16-22 are separately patentable, as the Office Action provides no specific basis for the rejections of these claims and because Ooishi does not disclose or suggest the detailed recitations of these claims. For example, nowhere does the Office Action indicate where Ooishi teaches or suggests the following recitations of Claim 7:

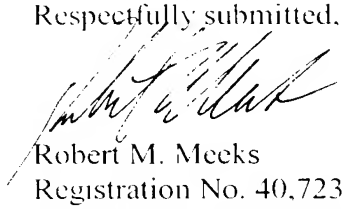
> . . . wherein a defective column select line in a first block of a predetermined input output block is replaced with any one of a spare column select line in the first block of the predetermined input output block, a spare column select line in a second block of the predetermined input output block, and a spare column select line in a second block in an input/output block adjacent to the predetermined input/output block.

Applicant submits that the Office Action is similarly deficient in providing basis for rejection of several other of the dependent claims, and defers further detailed discussion of these claims pending provision of a more specific indication as to where the cited reference allegedly teaches the recitations of these claims.

CONCLUSION

Applicant has amended Claims 20-22 to correct the inadvertent antecedent basis error noted by the Examiner. Applicant respectfully traverses the rejections of based on Ooishi because, among other reasons, this reference describes a memory with an entirely different input output configuration than that recited in the claims. Applicant respectfully submits that the claims are now in condition for allowance, and requests allowance of the claims and passing of the application to issue in due course.

Respectfully submitted,



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